

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Leonard Forbes et al.

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CIRCUITS WITH A TRENCH CAPACITOR HAVING MICRO-ROUGHENED

SEMICONDUCTOR SURFACES

Docket No.: 303.389US2

Serial No.: 09/467992

Filed:

December 20, 1999

Due Date: March 16, 2004

Examiner:

Eugene Lee

Group Art Unit: 2815

MS Non-Fee Amendment

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

We are transmitting herewith the following attached items (as indicated with an "X"):

X A return postcard.

- X An Amendment and Response (13 Pages).
- X A Communication Concerning Related Applications (7 pgs.).
- X Formal Drawings (5 pgs.).
- X A copy of the Preliminary Amendment filed October 9, 2003 (with returned PTO stamped postcard) (13 pgs.).

Please consider this a PETITION FOR EXTENSION OF TIME for sufficient number of months to enter these papers and please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

Customer Number 21186

Atty: Viet V. Tong Reg. No. 45,416

<u>CERTIFICATE UNDER 37 CFR 1.8:</u> The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: MS Non-Fee Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this <u>16th</u> day of March, 2004.

Name

Signature

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

(GENERAL)

<u>S/N 09/467992</u> <u>PATENT</u>

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Leonard Forbes et al.

Examiner: Eugene Lee

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CIRCUITS WITH A TRENCH CAPACITOR HAVING MICRO-ROUGHENED

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COMMUNICATION CONCERNING RELATED APPLICATION(S)

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Applicants would like to bring to the Examiner's attention the following related application(s) in the above-identified patent application:

Serial/Patent No. 08/889463 6072209	Filing Date July 8, 1997	Attorney Docket 303.322US1	Title FOUR F2 FOLDED BIT LINE DRAM CELL STRUCTURE HAVING BURIED BIT AND WORD LINES
09/527981 6689660	March 17, 2000	303.322US2	FOUR F2 FOLDED BIT LINE DRAM CELL STRUCTURE HAVING BURIED BIT AND WORD LINES
09/571352 6476434	May 16, 2000	303.322US3	FOUR F2 FOLDED BIT LINE DRAM CELL STRUCTURE HAVING BURIED BIT AND WORD LINES
08/889395 6191470	July 8, 1997	303.323US1	SEMICONDUCTOR-ON-INSULATOR MEMORY CELL WITH BURIED WORD AND BODY LINES
09/510095 6465298	February 22, 2000	303.323US2	SEMICONDUCTOR-ON-INSULATOR MEMORY CELL WITH BURIED WORD AND BODY LINES
08/889462 6150687	July 8, 1997	303.328US1	MEMORY CELL HAVING A VERTICAL TRANSISTOR WITH BURIED SOURCE/DRAIN AND DUAL GATES

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MEMORY CELL HAVING A August 24, 303.328US2 09/139164 VERTICAL TRANSISTOR WITH 6350635 1998 BURIED SOURCE/DRAIN AND DUAL **GATES** MEMORY CELL HAVING A 09/596266 June 16, 303.328US3 VERTICAL TRANSISTOR WITH 6399979 2000 BURIED SOURCE/DRAIN AND DUAL **GATES** MEMORY CELL HAVING A 09/651199 August 30, 303.328US4 VERTICAL TRANSISTOR WITH 2000 6504201 BURIED SOURCE/DRAIN AND DUAL **GATES** METHOD OF MAKING MEMORY July 8, 1997 303.329US1 08/889396 CELL WITH VERTICAL TRANSISTOR 5909618 AND BURIED WORD AND BODY LINES MEMORY CELL WITH VERTICAL 09/031620 February 303.329US2 TRANSISTOR AND BURIED WORD 6104061 27, 1998 AND BODY LINES MEMORY CELL WITH VERTICAL 09/520649 March 7, 303.329US3 TRANSISTOR AND BURIED WORD 6191448 2000 AND BODY LINES MEMORY CELL WITH VERTICAL 09/789274 February 303.329US4 TRANSISTOR AND BURIED WORD 6492233 20, 2001 AND BODY LINES 08/889554 July 8, 1997 303.330US1 ULTRA HIGH DENSITY FLASH **MEMORY** 5973356 A METHOD FOR FORMING HIGH 09/035304 303.330US2 February DENSITY FLASH MEMORY 6238976 27, 1998 ULTRA HIGH DENSITY FLASH 09/866938 303.330US3 May 29, 2001 **MEMORY** July 8, 1997 HIGH DENSITY FLASH MEMORY 08/889553 303.342US1 5936274

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09/137328 6143636	August 20, 1998	303.342US2	HIGH DENSITY FLASH MEMORY
08/939742 6066869	October 6, 1997	303.379US1	CIRCUIT AND METHOD FOR A FOLDED BIT LINE MEMORY CELL WITH VERTICAL TRANSISTOR AND TRENCH CAPACITOR
09/551027	April 17, 2000	303.379US2	CIRCUIT AND METHOD FOR A FOLDED BIT LINE MEMORY CELL WITH VERTICAL TRANSISTOR AND TRENCH CAPACITOR
08/944890 6528837	October 6, 1997	303.380US1	CIRCUIT AND METHOD FOR AN OPEN BIT LINE MEMORY CELL WITH A VERTICAL TRANSISTOR AND TRENCH PLATE TRENCH CAPACITOR
09/143606 6156604	August 31, 1998	303.380US2	METHOD FOR MAKING AN OPEN BIT LINE MEMORY CELL WITH A VERTICAL TRANSISTOR AND TRENCH PLATE TRENCH CAPACITOR
09/730245 6610566	December 5, 2000	303.380US3	CIRCUIT AND METHOD FOR AN OPEN BIT LINE MEMORY CELL WITH A VERTICAL TRANSISTOR AND TRENCH PLATE TRENCH CAPACITOR
09/010729 6025225	January 22, 1998	303.389US1	CIRCUITS WITH A TRENCH CAPACITOR HAVING MICRO- ROUGHENED SEMICONDUCTOR SURFACES AND METHODS FOR FORMING THE SAME
08/944312 5914511	October 6, 1997	303.391US1	CIRCUIT AND METHOD FOR A FOLDED BIT LINE MEMORY USING TRENCH PLATE CAPACITOR CELLS WITH BODY BIAS CONTACTS

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METHOD FOR A FOLDED BIT LINE August 24, 303.391US2 09/138796 MEMORY USING TRENCH PLATE 1998 6156607 CAPACITOR CELLS WITH BODY **BIAS CONTACTS** CIRCUIT AND METHOD FOR AN 08/939732 October 6, 303.393US1 1997 OPEN BIT LINE MEMORY CELL WITH 5907170 A VERTICAL TRANSISTOR AND TRENCH PLATE TRENCH **CAPACITOR** CIRCUIT AND METHOD FOR AN August 24, 303.393US2 09/138794 1998 OPEN BIT LINE MEMORY CELL WITH 6165836 A VERTICAL TRANSISTOR AND TRENCH PLATE TRENCH **CAPACITOR** CIRCUIT AND METHOD FOR AN December 303.393US3 09/742568 OPEN BIT LINE MEMORY CELL WITH 6537871 20, 2000 A VERTICAL TRANSISTOR AND TRENCH PLATE TRENCH CAPACITOR VERTICAL BIPOLAR READ ACCESS 09/028249 February 303.399US1 24, 1998 FOR LOW VOLTAGE MEMORY CELL 5963469 VERTICAL BIPOLAR READ ACCESS 09/328074 June 8, 303.399US2 1999 FOR LOW VOLTAGE MEMORY CELL 6317357 303.405US1 PROGRAMMABLE MEMORY 09/031621 February 27, 1998 ADDRESS DECODE ARRAY WITH 5991225 **VERTICAL TRANSISTORS** PROGRAMMABLE MEMORY 09/313049 May 17, 303.405US2 1999 ADDRESS DECODE ARRAYS WITH 6153468 VERTICAL TRANSISTOR 09/669281 September 303.405US3 PROGRAMMABLE MEMORY 26, 2000 6597037 ADDRESS DECODE ARRAYS WITH VERTICAL TRANSISTOR

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09/032617 6124729	February 27, 1998	303.406US1	FIELD PROGRAMMABLE LOGIC ARRAYS WITH VERTICAL TRANSISTORS
09/520494 6486027	March 8, 2000	303.406US2	FIELD PROGRAMMABLE LOGIC ARRAYS WITH VERTICAL TRANSISTORS
09/129047 6208164	August 4, 1998	303.407US1	PROGRAMMABLE LOGIC ARRAY WITH VERTICAL TRANSISTORS
09/756089 6515510	January 8, 2001	303.407US2	PROGRAMMABLE LOGIC ARRAY WITH VERTICAL TRANSISTORS
09/756099 6486703	January 8, 2001	303.407US3	PROGRAMMABLE LOGIC ARRAY WITH VERTICAL TRANSISTORS
09/128848 6134175	August 4, 1998	303.408US1	MEMORY ADDRESS DECODE ARRAY WITH VERTICAL TRANSISTORS
09/650600 6498065	August 30, 2000	303.408US2	MEMORY ADDRESS DECODE ARRAY WITH VERTICAL TRANSISTORS
09/028805 6242775	February 24, 1998	303.410US1	CIRCUITS AND METHODS USING VERTICAL, COMPLEMENTARY TRANSISTORS
09/514493 6294418	February 29, 2000	303.410US2	CIRCUITS AND METHODS USING VERTICAL, COMPLEMENTARY TRANSISTORS
09/028807 6246083	February 24, 1998	303.412US1	VERTICAL GAIN CELL AND ARRAY FOR A DYNAMIC RANDOM ACCESS MEMORY AND METHOD FOR FORMING THE SAME
09/879592	June 12, 2001	303.412US2	VERTICAL GAIN CELL AND ARRAY FOR A DYNAMIC RANDOM ACCESS MEMORY AND METHOD FOR FORMING THE SAME

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10/305549

November

26, 2002

303.408US3

MEMORY ADDRESS DECODE

ARRAY WITH VERTICAL

TRANSISTORS

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VERTICAL GAIN CELL AND ARRAY 303.412US3 09/879602 June 12, FOR A DYNAMIC RANDOM ACCESS 6680864 2001 MEMORY AND METHOD FOR FORMING THE SAME CIRCUITS AND METHODS FOR A 09/028727 **February** 303.462US1 24, 1998 STATIC RANDOM ACCESS MEMORY 6304483 USING VERTICAL TRANSISTORS CIRCUITS AND METHODS FOR A 303.464US1 09/060048 April 14, MEMORY CELL WITH A TRENCH 1998 6043527 PLATE TRENCH CAPACITOR AND A VERTICAL BIPOLAR READ DEVICE CIRCUITS AND METHODS FOR A 09/498433 February 4, 303.464US2 2000 MEMORY CELL WITH A TRENCH 6381168 PLATE TRENCH CAPACITOR AND A VERTICAL BIPOLAR READ DEVICE CIRCUITS AND METHODS FOR A 09/916759 July 27, 303.464US3 6429065 2001 MEMORY CELL WITH A TRENCH PLATE TRENCH CAPACITOR AND A VERTICAL BIPOLAR READ DEVICE 09/916769 July 27, 303.464US4 CIRCUITS AND METHODS FOR A 2001 MEMORY CELL WITH A TRENCH 6418050 PLATE TRENCH CAPACITOR AND A VERTICAL BIPOLAR READ DEVICE CIRCUITS AND METHODS FOR A 09/916768 July 27, 303.464US5 2001 MEMORY CELL WITH A TRENCH 6434041 PLATE TRENCH CAPACITOR AND A VERTICAL BIPOLAR READ DEVICE 10/230244 August 28, 303.406US3 FIELD PROGRAMMABLE LOGIC 2002 ARRAYS WITH VERTICAL **TRANSISTORS**

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CIRCUIT AND METHOD FOR AN 303.380US4 10/361986 February OPEN BIT LINE MEMORY CELL WITH 11, 2003 A VERTICAL TRANSISTOR AND TRENCH PLATE TRENCH **CAPACITOR** VERTICAL GAIN CELL AND ARRAY December 303.412US4 10/738449 FOR A DYNAMIC RANDOM ACCESS 16, 2003 MEMORY AND METHOD FOR FORMING THE SAME Respectfully submitted, LEONARD FORBES ET AL. By Applicants' Representatives,

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<u>CERTIFICATE UNDER 37 CFR 1.8:</u> The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this <u>16th</u> day of <u>March</u>, 2004.

Name

Hmy moriarty

Signature